power corresponding load **106**, and to also power load-switcher circuitry **215**. Control circuitry **102** further controls load-switcher circuitry **215** via control signals **203** to power load **116**. Thus, system **200** includes a single voltage regulator providing power to load **106** and load-switcher circuitry **215**—which replaces voltage regulator **115** of system **100** to provide power to load **116**.

[0015] Load-switcher circuitry generally include one or more transistors, such as a Field Effect Transistor (FET), which may be implemented, for example, as a metal oxide semiconductor FET (MOSFET). In load-switcher circuitry topologies, the MOSFET component may occupy a relatively large portion of the area of the load-switcher circuitry. Thus, it may be desired to minimize the relative size of the MOSFET in the load-switcher circuitry. As would be understood by one of skill in the art, a physical MOSFET coupled in a circuit empirically has a source-drain resistance and three parasitic capacitances: a parasitic capacitance between source and drain, a parasitic capacitance between gate and drain, and a parasitic capacitance between gate and source. A physical MOSFET will have voltages corresponding to each of the parasitic capacitances. Gate-source voltage fluctuations and the maximum values thereof strain a MOSFET, and the MOSFET must be sized large enough to handle maximum gate-source voltage swings.

[0016] Thus, to minimize the size of the MOSFET component of load-switcher circuitry it is desired to reduce the voltage stress on the MOSFET by controlling the voltage and power applied to the MOSFET in the load-switcher circuitry. Furthermore, there is a correlation between the source-drain resistance and the voltage applied to the MOSFET: the higher the voltage applied, the higher the relative source-drain resistance, and inversely, the lower the voltage applied, the lower the relative source-drain resistance.

[0017] The Miller effect may be leveraged to reduce the voltage stress on the MOSFET by controlling the voltage and power applied to the MOSFET in the load-switcher circuitry. To this end, an external buffer may be connected between drain and gate to control the MOSFET on/off speed. Further, a slow gate charge circuit may be implemented in the load switcher circuitry relative to the MOSFET (and the gate of the MOSFET), to control gate-source voltage parameters of the MOSFET.

[0018] Still further, voltage stress on the MOSFET may be reduced by controlling the timing of applying a voltage supply to the MOSFET. For example, the supply voltage could be applied to the MOSFET at an earlier time than otherwise. Thus, an external buffer, a slow gate charge circuit, and controlled temporal application of the supply voltage to a MOSFET may be used to reduce the voltage stress on the MOSFET.

[0019] FIG. **3***a* illustrates an example of load-switcher circuitry **300***a* utilizing a MOSFET **310**. Load-switcher circuitry **300***a* includes load **320** (illustrated as a resistor to indicate power loss) and voltage supply **322**, which corresponds to the voltage output of voltage regulator **105** of system **200**. As illustrated, the drain of MOSFET **310** is coupled to load **320**. As illustrated, voltage supply **322** is coupled to the source of MOSFET **310** via switch **323** which may be opened or closed to connect or disconnect the voltage output of voltage supply **322** with the source of MOSFET **310**.

[0020] Resistor **332** and capacitor **334** form a buffer or part of a buffer to control MOSFET **310** on/off speed. Resistor **332** and capacitor **334** are connected in series (between gate and drain). As illustrated, capacitor **334** is connected to the gate of MOSFET **310** and resistor **332** is connected to the drain of MOSFET **310**. Resistors **344** and **346** together with switch **345** form a slow gate charge circuit or part of a slow gate charge circuit. Control voltage **342** corresponds to control signals **203** of system **200** and is connected to the gate of MOSFET **310** via resistors **344** and **346**, which are connected in series. One end of resistor **344** is coupled to control voltage **342**, while the antipodal end of resistor **344** is coupled to switch **345** which is configured to be operable to short the voltage output of control voltage **342** to ground via resistor **344**, thereby allowing for controlled application of voltage from control voltage **342** to control the gate of MOSFET **310**. Resistor **346** is coupled to the antipodal end of resistor **344**, and to the gate of MOSFET **310**, thereby coupling resistor **344** to the gate.

[0021] Turning to MOSFET **310**, MOSFET **310** has a source, drain, and controlling gate, as labeled in system **300***a*. As illustrated, MOSFET **310** is a p-type FET with an active-off gate control voltage. MOSFET **310** has an inherent resistance from source to drain, illustrated as resistor **311**. MOSFET **310** further has parasitic capacitances **312**, **314**, and **316**. Capacitance **312** is the parasitic capacitance between gate and source. Capacitance **314** is the parasitic capacitance between gate and drain. And capacitance **316** is the parasitic capacitance between drain and source.

[0022] The respective resistances of resistors **344** and **346** are selected for charging and discharging parasitic capacitances **312** and **314** (the parasitic capacitances associated with the gate of MOSFET **310**). More particularly, since resistors **344** and **346** are in series between the gate of MOSFET **310** and control voltage **342**, the effective resistance of the combination of resistors **344** and **346** slow the application of voltage from control voltage **342** to the gate of MOSFET **310**, thereby slowing the charging of capacitances **312** and **314** by control voltage **342**. Switch **345** uses shorting control voltage **342** to control the application of voltage from control voltage **342** to the gate of MOSFET **310**. When switch **345** is electrically connected to ground, parasitic capacitances **312** and **314** discharge through resistor **346** to ground.

[0023] More particularly, when switch **345** is operated to disconnect resistor **344** from ground, control voltage **342** is electrically coupled to the gate of MOSFET **310** via resistors **344** and **346**, and the voltage of control voltage **342** charges capacitances **312** and **314**, as well as capacitor **334** (allowing for the resistance values of resistors **344** and **346** to affect a rate of charge of capacitances **312** and **314**). Furthermore, since capacitor **334** is also simultaneously charging along with charging capacitances **312** and **314**, the capacitance value of capacitor **334** affects the rate of charge of capacitances **312** and **314**.

[0024] Conversely, when switch **345** is operated to connect resistor **344** to ground, control voltage **342** is electrically decoupled from the gate of MOSFET **310** because control voltage **342** is shorted to ground via resistor **344**. Furthermore, when switch **345** is operated to connect resistor **344** to ground, as illustrated in FIG. **3***a*, one end of resistor **346** will also be shorted to the ground, and parasitic capacitances **312** and **314** will be connected to ground, and charge from parasitic capacitances **312** and **314** will flow to